1 Device Overview

RFA1810 is a wireless Transceiver for battery powered Low Power application. It typically operates in the unlicensed radio spectrum in the Industrial, Scientific and Medical (ISM) band.

1.1 Key Features

- Fully integrated transceiver
- RF Frequency range 137MHz to 1050MHz
- GFSK/GMSK/OOK modem
- Excellent Receiver Sensitivity -125dBm
- RF output power 5dBm for LP mode and 20dBm for HP mode
- Programmable bit rate from 0.5 to 350Kbps
- RSSI -127dBm
- Power supplied by 1.5V or 3.0V battery, super low power consumption
- compatible with IEEE802.15.4G specification

1.2 Applications

- Smart grid and automatic meter reading
    a. Water, gas, and electricity meters
    b. Heat cost allocators
- Wireless sensor networks
- Industrial
    a. Asset tracking
    b. Factory automation
- Home and building automation
    a. Electronic Shelf Labeling
    b. Wireless alarm and security
    c. Locks
    d. Garage door control
    e. Connected appliance
- Long range irrigation system
- Control and monitoring
- Other IOT applications

1.3 Package and Operating Temperature

- QFN 16 pins 3mm x 3mm package
- -40 ~ 85 °C operating temperature range

2 Specification

2.1 FSK mode

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage Range		1.3	1.5	3.7	V
Supply Current in Sleep mode		0.3	0.5	1.0	uA
Supply Current in receive mode		-	6.0	-	mA
Supply Current in transmit mode	HP mode	-	75.0	-	mA
Frequency Range		137.0	-	1050.0	MHz
Bit Rate		0.1	-	350.0	Kbps
RF sensitivity 1	at RX BR = 0.5Kbps	-	-125	-	dBm
RF sensitivity 2	at RX BR = 100Kbps	-	-103	-	dBm
Channel Bandwidth		1	200.0	500	KHz
Input IP3			-11.0		dBm
Input IP2			55.0		dBm
Adjacent Channel Rejection	Channel spacing = 12.5 KHz		58		dB
Blocking Immunity	1MHz offset		75		dB
Image Rejection			55		dB
RSSI Dynamic Range		-127.0		0.0	dBm
RF Output Power (LP mode)		4.0	5.0	6.0	dBm
RF Output Power (HP mode)		19.0	20.0	21.0	dBm
Transmitter Phase Noise	470MHz, 400KHz offset		-122.0		dBc/Hz
Crystal Oscillator Frequency			32.0		MHz

3 Descriptions

3.1 Functional Block Diagram

RFA1810 is shown on fig 1

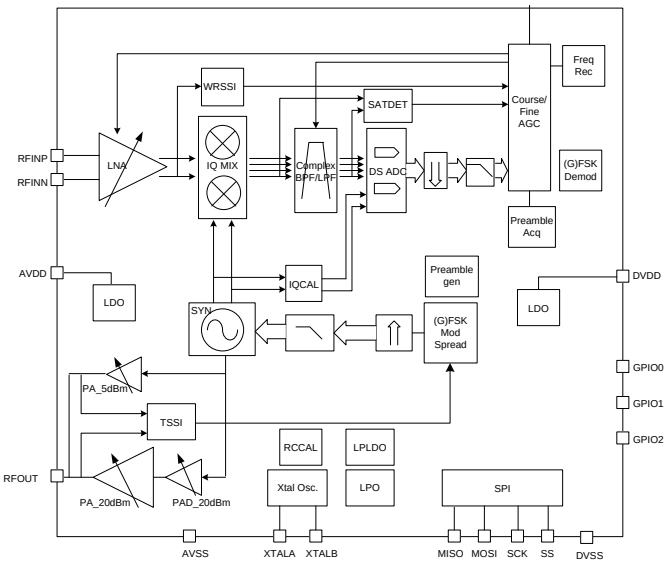


Fig 1 Simplified Block Diagram

3.2 Radio

RFA1810 PHY transceiver adopts a half-duplex, low-IF/zero-IF architecture. The received RF signal is first amplified by the LNA and then down-converted to in-phase and quadrature (I&Q) components by I&Q mixers. Only one set of LNA and mixers are employed to handle different frequency bands with associated different off-chip LC networks. A configurable complex band pass filter/LPF is used to channel select the desired IF signal and followed by a pair of continuous delta-sigma ADCs to perform data conversion. The following decimation and low pass filtering are done in the digital domain. WRSSI and Saturation Detector are used to monitor the signal strength and output to AGC block.

The frequency synthesizer utilizes only one wide tuning range VCO and different divider ratio to generate the required LO frequency. The PLL is designed with fast locking and auto-CAL features. In transmission, the frequency modulation is performed digitally within the PLL bandwidth.

Two PAs, one for LP mode and the other for HP mode, are designed for different purposes. LP mode PA is operated with low battery voltage and low current, which is good for low BOM cost and shorter communication distance applications. HP mode PA, on the other hand, with the cost of more power consumption, can cover wider communication areas.

3.3 Controller Interface

The transceiver integrates standard 4 wire SPI interface to communicate with host controller. In addition, it provides a number of GPIO ports which are functionally reconfigurable for general user purposes. With host controller, the transceiver can be

It supports the operation mode (Table below) that is compatible with IEEE802.15.4G specification

Number	State	Description
1	SLEEP	Sleep mode, very low power consumption
2	STNDBY	Standby mode
3	PLL_TX	Frequency synthesizer tune to TX frequency
4	TX	Transmit
5	PLL_RX	Frequency synthesizer tune to RX frequency
6	RX	Receive

Sleep mode is the lowest current consumption state of the device with nominally less than 30 nA of current consumption. Standby state has the lowest current consumption with the exception of shutdown but has much faster response time to RX or TX mode. In most cases standby should be used as the low power state. In this state the register values are maintained with all other blocks disabled. The SPI is accessible during this mode but any SPI event.

PLL state is designed to give a fast transition time to TX or RX state with reasonable current consumption. In this mode the Crystal oscillator remains enabled reducing the time required to switch to TX or RX mode by eliminating the crystal start-up time.

The TX state may be entered from any of the state with the “Start TX” or “Change State” API commands. A built-in sequencer takes care of all the actions required to transition between states from enabling the crystal oscillator to ramping up the PA. The RX state may be entered from any of the other states by using the “Start RX” or “Change State” API command. A built-in sequencer takes care of all the actions required to transition between states.

3.4 Modem

RFA1810 is especially suited to narrow band communications that support both zero and low IF architecture. When operating in GFSK/GMSK/OOK mode, it is compatible to IEEE802.15.4g for operation flexibility

The receiver includes channel filters, AGC, AFC, digital mixer, interleaver, FEC etc. For GFSK/GMSK modem, coherent and noncoherent modulation can be configured. Coherent mode gives better performance when GFSK/GMSK modulation index is less than 2; Noncoherent demodulation get better performance for modulation index is above 2.

Signal bandwidth for each channel is configurable. Wide signal bandwidth permits the use of a higher effective data rate; while narrow bandwidth save spectrum with lower data rate. The digital mixer is used for frequency-phase recovery.

RFA1810 modem uses error correction code.

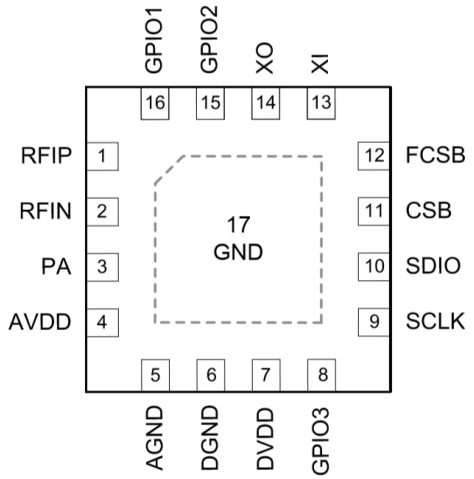
For data whiting, IEEE802.15.4g scrambler is used. It's LFSR polynomial is

$$Y = X^8 + X^4 + X^3 + X^2 \qquad \text{(Eq. 1)}$$

3.5 Packet Structure

The general packet structure contains 1-255 bytes of preamble, 1-4 bytes of sync word, 0-4 bytes of header, payload, and CRC

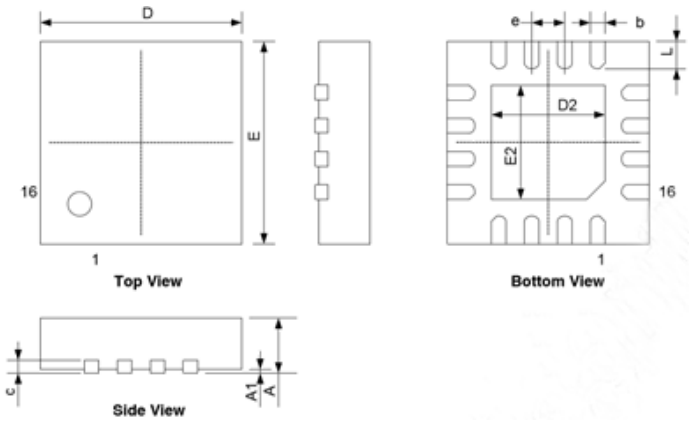
4 Pin Configurations



Pin #	Pin Name	I/O	Function Description
1	RFIP	I	RF input differential P
2	RFIN	I	RF input differential N
3	PAOUT	O	PA output
4	AVDD	IO	Analog VDD
5	AGND	IO	Analog GND
6	DGND	IO	Digital GND
7	DVDD	IO	Digital VDD
8	GPIO3	IO	Can be configured to: CLKO, DOUT/DIN, INT2, DCLK(TX/RX)
9	SCLK	I	SPI CLK
10	SDIO	IO	SPI Data I/O
11	CSB	I	SPI Reg Enable
12	FCSB	I	SPI FIFO Enable
13	XI	I	Crystal In
14	XO	O	Crystal Out
15	GPIO2	IO	Can be configured to: INT1, INT2, DOUT/DIN, DCLK(TX/RX), RF_SWT
16	GPIO1	IO	Can be configured to: DOUT/DIN, INT1, INT2, DCLK(TX/RX), RF_SWT
17	GND	I	Analog GND

5 Package Information

The QFN 16 pins 3mm x 3mm package is shown below:



Symbol	Dimention (mm)	
	Min	Max
A	0.7	0.8
A1	N/A	0.05
b	0.18	0.3
c	0.18	0.25
D	2.9	3.1
D2	1.55	1.75
e	0.5 BSC	
E	2.9	3.1
E2	1.55	1.75
L	0.35	0.45

Contact

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